

coupling a second resistor to the second cascode transistor, the amplified second signal being provided between the second resistor and the second cascode transistor.

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19. (Amended) The method of claim [18] 16, wherein the step of [connecting] coupling the second capacitor and the second active element in [parallel with the second capacitor] series between the second input signal node and the first amplifier transistor comprises:

connecting a control element of the second active element to the second input signal node; and

connecting a controlled element of the second active element to a control element of the first amplifier transistor.

20. (Amended) The method of claim [17] 16, wherein the step of [connecting] coupling the first capacitor and the first active element in [parallel with the first capacitor] series between the first input signal node and the second amplifier transistor comprises:

connecting a control element of the first active element to the first input signal node; and

connecting a controlled element of the first active element to a control element of the second amplifier transistor.

REMARKS

This Amendment is in response to the Office Action mailed on March 12, 2003, in which claims 1-20 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art in view of U.S. Patent No. 5,559,646 to Voorman et al.

The present invention is a differential amplifier circuit for amplifying an input signal and for providing an output signal representative of the input signal. By implementing the differential amplifier circuit of the present invention, a cross-coupled input stage is provided with

improved bandwidth and high frequency noise performance. In contrast to prior art differential amplifier circuits, the present invention includes first and second coupling circuits each including a capacitor and an active element coupled in series between an input signal node and an input transistor. By implementing coupling circuits that include a capacitor and an active element coupled in series, the present invention provides a reduced net capacitance (because two capacitances are connected in series) between the input signal nodes and the input transistors. The reduced effective input capacitances extend the upper cutoff frequencies of the input transistors, and increase the bandwidth of the differential amplifier circuit. This results in reduced high frequency noise, and greater accuracy and capability in detecting data recorded on a magnetic disk.

U.S. Patent No. 5,559,646 to Voorman et al. discloses an arrangement for reading out an information signal from a magnetic record carrier. The Voorman et al. patent does not disclose, teach or suggest a differential amplifier circuit comprising first and second coupling circuits each including a capacitor and an active element coupled in series between an input signal node and an input transistor, as recited in the pending claims, as amended. Instead, the Voorman et al. patent simply discloses the use of a capacitor (C1 or C2) coupled between an input terminal (7 or 67) and an input transistor (T1 or T2). This is the same configuration that is disclosed as prior art in FIG. 3 of the above-identified application. The Voorman et al. patent also discloses (as prior art in FIG. 1) the use of a feedback circuit (F1 or F2) coupled between an input transistor (T1 or T2) and an output terminal (8 or 68) within the same amplifier circuit. This is quite different from coupling an input terminal of one amplifier circuit to an input transistor of another amplifier circuit. Moreover, this has nothing to do with reducing the net capacitance between an input terminal of one amplifier circuit and an input transistor of another amplifier circuit (by connecting two capacitances in series) to lead to a higher upper cutoff frequency. In fact, Examiner correctly points out that the motivation of using a feedback circuit (F1 or F2) in the Voorman et al. patent is to add high-ohmic impedance to obtain a desired value for the lower cutoff frequency (col. 5 lines 14-21). Therefore, the Voorman et al. patent, either along or in combination with the admitted prior art, falls short of meeting the requirements of the present invention.

Independent claims 1, 6, 11, 13 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of U.S. Patent No. 5,559,646 to Voorman et al. With this Amendment, claims 1, 6 and 14 have been amended to clarify that the capacitor and the active element are coupled in series. Because AAPA and the Voorman et al. patent together do not disclose, teach or suggest all of the recited elements of amended claims 1, 6 and 14 and claims 11 and 13, the rejection of claims 1, 6, 11, 13 and 14 under 35 U.S.C. § 103 should be withdrawn. Reconsideration and allowance of claims 1, 6, 11, 13 and 14 are respectfully requested.

Claims 2-5 depend from amended claim 1, and are allowable therewith. Reconsideration and allowance of claims 2-5 are respectfully requested.

Claims 7-10 depend from amended claim 6, and are allowable therewith. Reconsideration and allowance of claims 7-10 are respectfully requested.

Claim 12 depends from independent claim 11, and is allowable therewith. Reconsideration and allowance of claim 12 are respectfully requested.

Claims 15, 16, 19 and 20 depend from amended claim 14, and are allowable therewith. Reconsideration and allowance of claims 15, 16, 19 and 20 are respectfully requested.

Claims 17 and 18 have been canceled without prejudice, thereby rendering moot their rejection.

CONCLUSION

In view of the foregoing, all pending claims 1-16, 19 and 20 are now in condition for allowance. Notice to that effect is respectfully requested.

The Commissioner is authorized to charge any additional fees associated with this paper or credit any overpayment to Deposit Account No. 11-0982. A duplicate copy of this communication is enclosed.

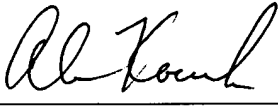
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Respectfully submitted,

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**APPENDIX:
MARKED UP VERSION OF CLAIM AMENDMENTS**

- 1.(Amended) A differential amplifier circuit for amplifying an input signal and for providing an output signal representative of the input signal, the differential amplifier circuit comprising:
first and second input signal nodes;
a first amplifier circuit including an input transistor operatively connected to the first input signal node;
a second amplifier circuit including an input transistor operatively connected to the second input signal node;
a first coupling circuit including a capacitor and an active element, the first coupling circuit being connected such that the capacitor and the active element are coupled in series between the first input signal node and the input transistor of the second amplifier circuit; and
a second coupling circuit including a capacitor and an active element, the second coupling circuit being connected such that the capacitor and the active element are coupled in series between the second input signal node and the input transistor of the first amplifier circuit.
2. (Amended) The differential amplifier circuit of claim 1 wherein the input transistors of the first and second amplifier circuits each have a base, a collector and an emitter, and the first and second amplifier circuits each include:
[an input transistor having a base, a collector, and an emitter;]
a collector circuit connected between a fixed potential and the collector of the input transistor; and
a current generator for directing current through the input transistor and the collector circuit.
- 6.(Amended) A read system for reading information from a magnetic storage medium using a magnetoresistive head and for providing an output signal representative of the information read, the read system comprising:
first and second input signal nodes for connection to the magnetoresistive head;
a first amplifier circuit including an input transistor operatively connected to the first input signal node;
a second amplifier circuit including an input transistor operatively connected to the second input signal node;
a first coupling circuit including a capacitor and an active element, the first coupling circuit being connected such that the capacitor and the active element are coupled in series between the first input signal node and the input transistor of the second amplifier circuit; and
a second coupling circuit including a capacitor and an active element, the second coupling circuit being connected such that the capacitor and the

**APPENDIX:
MARKED UP VERSION OF CLAIM AMENDMENTS**

active element are coupled in series between the second input signal node and the input transistor of the first amplifier circuit.

7. (Amended) The read system of claim 6 wherein the input transistors of the first and second amplifier circuits each have a base, a collector and an emitter, and the first and second amplifier circuits each include:

[an input transistor having a base, a collector, and an emitter;]
a collector circuit connected between a fixed potential and the collector of the input transistor; and
a current generator for directing current through the input transistor and the collector circuit.

14.(Amended) A method of amplifying an input signal from a magnetoresistive head, the input signal comprising a differential signal including a first signal provided at a first input signal node and a second signal provided at a second input signal node, the first and second input signal nodes being connected to opposite sides of the magnetoresistive head, the method comprising:

amplifying the first signal with a first amplifier circuit to provide an amplified first signal;
amplifying the second signal with a second amplifier circuit to provide an amplified second signal;
coupling a first capacitor and a first active element in series between the first input signal node and the second amplifier circuit; and
coupling a second capacitor and a second active element in series between the second input signal node and the first amplifier circuit.

19. (Amended) The method of claim [18] 16, wherein the step of [connecting] coupling the second capacitor and the second active element in [parallel with the second capacitor] series between the second input signal node and the first amplifier transistor comprises:

connecting a control element of the second active element to the second input signal node; and
connecting a controlled element of the second active element to a control element of the first amplifier transistor.

20. (Amended) The method of claim [17] 16, wherein the step of [connecting] coupling the first capacitor and the first active element in [parallel with the first capacitor] series between the first input signal node and the second amplifier transistor comprises:

connecting a control element of the first active element to the first input signal node; and
connecting a controlled element of the first active element to a control element of the second amplifier transistor.